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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,892	01/21/2004	Tien-Jen Cheng	FIS920030352US1	1891

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BLDG. 300-482
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EXAMINER
LANDAU, MATTHEW C

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/707,892	CHENG ET AL.	
	Examiner	Art Unit	
	Matthew C. Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-14 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-14 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The declaration filed on November 6, 2007 under 37 CFR 1.131 is sufficient to overcome the Cheng et al. and Biggs et al. references cited in the previous Office Action.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "underlying chip wiring" with a terminal metal layer disposed on a chip passivating layer and connecting to underlying chip wiring through a via through said chip passivating layer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 8 is objected to because of the following informalities: the limitation "said diffusion barrier layer" lacks sufficient antecedent basis in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5, 7, 21, 22, and 25 are rejected under 35 U.S.C. 102(e)as being anticipated by Walker et al. (US Pat. 6,534,863, hereinafter Walker).

Regarding claims 1, 5, 7, 21, and 25, Figure 4C of Walker discloses a chip pad comprising: a terminal metal layer 27 disposed on a passivation layer 25 (low-k dielectric) (col. 4, lines 27-29); a diffusion barrier layer 22 on said terminal metal layer; a conducting layer pad 23 (Cu) (col. 4, lines 43 and 44) on said diffusion barrier; a hard test barrier layer 24 (Ni) (col. 4, lines 60-62) on, and enclosing, said conducting layer pad, wherein said hard test barrier layer

extends along the sides of said of said conducting layer pad and said conducting layer pad is completely enclosed by said diffusion layer and said hard test barrier layer, and a plate passivation layer 26 (Au) (col. 5, lines 3 and 4) on said hard test barrier layer.

Regarding claim 2 and 22, Figure 4C of Walker discloses the diffusion barrier layer includes an adhesion layer on barrier metallurgy (col. 4, lines 30-37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4, 23, and 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Walker in view of Lopatin (US Pat. 6,144,096).

Regarding claims 3, 4, 23, and 24, Walker discloses the barrier layer is made of TaN and the adhesion layer is made of Ta (col. 4, lines 34-37). Walker does not disclose the barrier and adhesion layers are made of materials selected from the list of materials claimed. Lopatin discloses a barrier/adhesion layer combo can be made of Ti/TiN or Ta/TaN (col. 2, lines 26-30). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Walker by using TiN as the barrier layer and Ti as the adhesion layer for the purpose of selecting equivalent materials known in the art to be used for the same purpose (see MPEP 2144.06).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walker.

Regarding claim 8, Figure 4C of Walker discloses a chip pad comprising: a terminal metal layer 27 disposed on a passivation layer 25 (low-k dielectric) (col. 4, lines 27-29) extended through a via in the passivation layer; an adhesion/barrier layer 22 on said terminal metal layer; a seed pad 23 (Cu) (col. 4, lines 43 and 44) on said diffusion barrier; a hard test barrier layer 24 (Ni) (col. 4, lines 60-62) on, and enclosing, said seed pad, wherein said hard test barrier layer extends along the sides of said of said seed pad and said seed pad is completely enclosed by said diffusion layer and said hard test barrier layer, and a plate passivation layer 26 (Au) (col. 5, lines 3 and 4) on said hard test barrier layer. Walker does not specifically disclose an IC chip with circuits formed therein, and a plurality of chip interconnect pads being on a surface of said IC chip. However, it would have been obvious to use the interconnect pad disclosed by Walker in an IC with a plurality of chip interconnect pads since such configurations are very well known in the art and allow for increased integration density while allowing separate electrical connections to different portions of the IC. Walker also does not explicitly disclose the terminal metal connecting to underlying chip wiring through the via. However, it would have been obvious, if not inherent, that the terminal metal layer connects to some type of circuit in a chip to impart a functionality to the interconnect and to allow for electrical connection to the internal circuits of an IC.

Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker as applied to claim 8 above, and further in view of Lopatin.

Regarding claims 9 and 10, Walker discloses the barrier layer is made of TaN and the adhesion layer is made of Ta (col. 4, lines 34-37). Walker does not disclose the barrier and adhesion layers are made of materials selected from the list of materials claimed. Lopatin discloses a barrier/adhesion layer combo can be made of Ti/TiN or Ta/TaN (col. 2, lines 26-30). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Walker by using TiN as the barrier layer and Ti as the adhesion layer for the purpose of selecting equivalent materials known in the art to be used for the same purpose (see MPEP 2144.06).

Regarding claims 11-13, the limitations of these claims are taught by Walker as indicated in the rejection of claim 8 above.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walker in view of Lopatin as applied to claim 13 above, and further in view of Homma et al. (US Pat. 6,798,050, hereinafter Homma) and Bhattacharya et al. (US PGPub 2003/0034489, hereinafter Bhatt).

Regarding claim 14, semiconductor IC chips are fabricated from a wafer of semiconductor material, and the wafer is not diced into individual chips until after the ICs have been completed. Therefore, in order to make the device of the above combination, there must have been a plurality of IC chips on a wafer at an intermediate stage of processing. However, Walker does not explicitly disclose that the wafer is diced into individual IC chips after forming the claimed metal layers on the IC chip substrate. Figures 9A-9E of Homma discloses forming a plurality of metal layers on a wafer prior to dicing the wafer into individual chips (col. 11, lines 38-41). In view of such teaching, it would have been obvious to the ordinary artisan at the time

the invention was made to further modify the invention of Walker by dicing the wafer after forming the claimed metal layers, thereby resulting in a plurality of ICs (with the claimed structure) on a wafer. The ordinary artisan would have been motivated to further modify Walker in the manner described above for the purpose of simply the production process for mass production. A further difference between Walker and the claimed invention is the ICs are identical. Bhatt discloses forming a plurality of identical ICs on a wafer (paragraph [0030]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Walker by having a plurality of identical ICs on a wafer for the purpose of simplifying the production process for mass production of a particular IC. Note that paragraph [0003] of the instant application gives a special definition to the word "die" by stating, "Each array location is known as a die and each die may harbor an IC chip". In other words, a "die" is simply the portion of the wafer where the chip is located. Therefore, it is inherent that each of said plurality of identical ICs are located in a die on said wafer.

Response to Arguments

Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is 571-272-1731. The examiner can normally be reached on 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew C. Landau
Primary Examiner
Art Unit 2815